(19) World Intellectual Property **Organization**

International Bureau



(43) International Publication Date 21 July 2005 (21.07.2005)

PCT

(10) International Publication Number WO 2005/067019 A1

(51) International Patent Classification⁷: H01L 21/302, C23F 1/02

(21) International Application Number:

PCT/US2004/043887

(22) International Filing Date:

30 December 2004 (30.12.2004)

(25) Filing Language:

English

(26) Publication Language:

English

US

(30) Priority Data:

60/533,097 30 December 2003 (30.12.2003)

(71) Applicant (for all designated States except US): AKRION, LLC [US/US]; 6330 Hedgewood Drive, Allentown, PA 18106 (US).

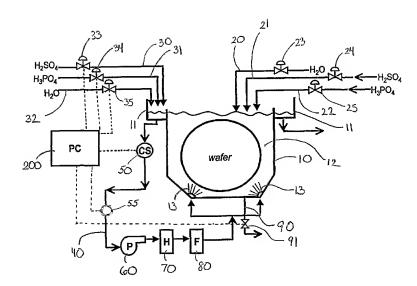
- (72) Inventors; and
- (75) Inventors/Applicants (for US only): KASHKOUSH, Ismail [US/US]; 5919 Ricky Ridge Trail, Orefield, PA 18069 (US). CHEN, Gim-Syang [US/US]; 192 Windermere Avenue, Allentown, PA 18104 (US). NOVAK,

Richard [US/US]; 2000 Fountain Lane, Plymouth, MN 55447 (US).

- (74) Agent: BELLES, Brian, L.; Cozen O'Connor, 1900 Market Street, Philadelphia, PA 19103 (US).
- (81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.
- (84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

[Continued on next page]

(54) Title: SYSTEM AND METHOD FOR SELECTIVE ETCHING OF SILICON NITRIDE DURING SUBSTRATE PROCESS-ING



(57) Abstract: A system (fig.5) and methods for selectively etching silicon nitride in the presence of silicon oxide that provide high selectivity while stabilizing silicon oxide etch rates. The invention comprises a processing chamber (10), dispense lines (20, 21, 22), feed lines (30, 31, 32), a recirculation line (40), a process controller (200), a concentration sensor (50), a particle counter (55), and a bleed line (90). The invention dynamically controls the concentration ratio of the components of the etchant being used and/or dynamically controls the particle count within the etchant during the processing of the at least one substrate. As a result etchant bath life is increased and etching process parameters are more tightly controlled.



Published:

with international search report

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.